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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,241	12/31/2003	Jeong Ho Park	09407.0001	6968

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,241	PARK, JEONG HO	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the RCE and amendment filed on. Currently, claims 13-23 are pending.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/06/06 has been entered.

Allowable Subject Matter

The indicated allowability of claims 13-23 are withdrawn in view of the newly discovered reference(s) to "anisotropically etching the first insulating layer to form spacers;" Rejections based on the newly cited reference(s) follow.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 13-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Azam et al., US Patent 6,753,228.

Azam discloses the semiconductor method as claimed. See figures 1-9 and corresponding text, where Azam teaches, pertaining to claim 13, a method for fabricating a semiconductor transistor, comprising: forming an LDD region **49** using an ion implantation in a substrate **15** (figure 8; col. 5, lines 64-67; col. 6, lines 1-11); forming a first insulating layer **42** on the substrate (figure 4; col. 4, lines 7-13); patterning the first insulating layer (figure 5; col. 4, lines 55-60); forming a trench **14** in the substrate (figure 2; col. 3, lines 20-33); forming a trench gate **17** by depositing and planarizing a second insulating layer **39** and a conductor on the substrate with the trench formed therein, the trench gate comprising the second insulating layer and the conductor; anisotropically etching the first insulating layer to form spacers (figures 4 and 5; col. 4, lines 61-64, ***Note***: the Examiner takes the position that an L-shaped spacer is anisotropically formed, since Azam teaches a dry-etching process to create the spacers); and forming source/drain regions **47** by performing an ion implantation on the substrate using the spacers and the trench gate as a mask (figure 6; col. 5, lines 10-23).

Azam teaches, pertaining to claim 14, further comprising performing a thermal process after forming the source/drain regions (figure 6, col. 5, lines 10-23).

Azam teaches, pertaining to claim 15, wherein the first insulating layer is an oxide layer or a nitride layer (col. 4, lines 19-24, nitride).

Azam teaches, pertaining to claim 16, wherein the conductor comprises one selected from the group consisting of polysilicon, tungsten alloys, titanium alloys, and tantalum alloys (col. 2, lines 35-38).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Azam et al., US Patent 6,753,228.

Azam discloses the semiconductor method substantially as claimed. See preceding rejection of claims 13-16 under 35 U.S.C. 102(e). In addition, Azam fails to show, pertaining to claim 21, wherein lower edges of the trench are in a rounded shape.

However, Azam fails to show, pertaining to claim 17, wherein the energy of the ion implantation for forming the LDD region is between 10 keV and 80 keV. In addition, Azam fails to show, pertaining to claim 18, wherein the energy of the ion implantation for forming the source/drain regions is between 10 keV and 100 keV. Also, Azam fails to show, pertaining to

claim 19, wherein the trench is formed by dry etching. Azam fails to show, pertaining to claim 20, wherein the trench is formed by a dry etching using an angle etching and chemical dry etching. In addition, Azam fails to show, pertaining to claim 22, wherein the chemical dry etching uses CF_4/O_2 or CHF_3/O_2. Finally, Azam fails to show, pertaining to claim 23, wherein planarizing a second insulating layer and a conductor comprises a CMP process using the first insulating layer as an etch-stop layer.

Azam teaches, the formation of the LDD regions and source/drain regions (figures 6 and 8). In addition, Azam teaches, that the trench can be formed by techniques that are well known to those skilled in the art (col. 3, lines 25-28).

Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the following steps of: wherein the energy of the ion implantation for forming the LDD region is between 10 keV and 80 keV; wherein the energy of the ion implantation for forming the source/drain regions is between 10 keV and 100 keV; wherein the trench is formed by dry etching; wherein the trench is formed by a dry etching using an angle etching and chemical dry etching; wherein the chemical dry etching uses CF_4/O_2 or CHF_3/O_2; wherein planarizing a second insulating layer and conductor comprises a CMP process using the first insulating layer as an etch-stop layer, in the method of Azam, pertaining to claims 17-23, according to the teachings of Azam, with the motivation that having the desired the energy of the ion implantation for the LDD regions and source/drain regions would result in routine experimentation, where one of ordinary skill in the art would be able to adjust the amount of energy produced to create a desired LDD and source/drain regions. In addition, forming a trench by dry etching is well

known to one of ordinary skill in the art, where dry etching is attractive for creating a trench wall profile, hence would result in routine experimentation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
May 10, 2006

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
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